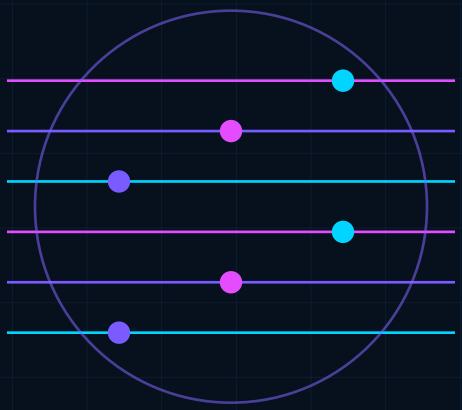
PHOTONICS AND INTERCONNECT

Silicon Photonics & Chip-to-Chip Optical Interconnects

Current-source review, evidence-bounded adoption decision, explicit limitations, reproducibility controls, and preserved source research note.



PERMANENT ID	EVIDENCE	ADOPTION	FRESHNESS
RES-020	A-	MONITOR AND PARTNER PILOT	STABLE WATCH

Freshness review: 2026-09-17 / Next scheduled review: 2027-03-16

RESEARCH CONTROL SURFACE

Required Research Fields

Each field remains independently reviewable; evidence strength does not imply production authority.

EVIDENCE GRADE **A-**

Strength of the retained source set and technical basis.

SOURCE AUTHORITY **1 registered authorities**

OIF Co-Packaging Implementation Agreements

FRESHNESS **STABLE WATCH**

Reviewed 2026-09-17; dynamic sources require event-driven revalidation.

CONFLICTS **VISIBLE / NOT SILENT**

Differences between specification, vendor behavior, research claims, and reproduced evidence must remain explicit.

LIMITATIONS **EXPLICIT**

No certification, procurement approval, legal conclusion, or unbounded production claim is created by this report.

REPRODUCIBILITY **REQUIRED**

Material claims require exact versions, representative data, failure cases, artifacts, and repeatable acceptance criteria.

ADOPTION POSTURE **MONITOR AND PARTNER PILOT**

Track silicon photonics and co-packaged optics as infrastructure roadmap inputs. Avoid production dependency until interoperability, thermal, serviceability, packaging, and supply-chain requirements are validated.

REVIEW TRIGGER **2027-03-16**

Scheduled at 180 days; earlier on material source, vulnerability, implementation, or contradictory-evidence change.

Authority Register and Freshness Delta

Primary-source lineage is preserved; current-source changes are separated from unperformed implementation claims.

AUTHORITY 01

OIF Co-Packaging Implementation Agreements

https://www.oiforum.com/technical-work/implementation-agreements-ia

2026-09-17 FRESHNESS DELTA

Primary-source register retained and freshness controls advanced to the current review date. No new product or laboratory performance claim is introduced without reproduced evidence.

Freshness policy: scheduled review + immediate review on source supersession, material release, vulnerability, retraction, or contradictory evidence.

Evidence Must Survive Contact With Reality

- Source authority is not implementation evidence. Product behavior, scale, security, interoperability, and operator fit remain environment-specific.
- Conflicting evidence is recorded rather than averaged away. Specification behavior, vendor implementation, preprint results, and production observations are separate evidence classes.
- Quantitative claims are informative until reproduced under documented hardware, software, data, topology, load, and failure conditions.
- Adoption posture is reversible. A stronger source set can coexist with a pilot-only or research-only recommendation when maturity, safety, economics, or operability remain unresolved.

ADOPTION / VALIDATION / REVIEW

Decision Gate and Validation Plan

ADOPTION POSTURE

MONITOR AND PARTNER PILOT

Track silicon photonics and co-packaged optics as infrastructure roadmap inputs. Avoid production dependency until interoperability, thermal, serviceability, packaging, and supply-chain requirements are validated.

1 / SOURCE	Pin exact versions, publication state, retrieved artifacts, and source hashes.
2 / PROTOTYPE	Demonstrate the core mechanism with representative data and instrumented execution.
3 / FAILURE	Exercise malformed input, dependency loss, stale state, overload, recovery, rollback, and misuse.
4 / BASELINE	Compare against an incumbent, classical, or simpler architecture using the same workload.
5 / ACCEPT	Record acceptance criteria, residual limitations, owner, expiration, and revalidation triggers.

EXPIRATION / REVIEW TRIGGER

Next scheduled review: 2027-03-16 (180-day cadence). Review sooner after material source revision, breaking implementation release, critical vulnerability, retraction, benchmark contradiction, changed workload, or changed legal/safety boundary.

- The Advantage: MRMs are incredibly small (microns in diameter) and consume femtojoules of energy per bit, enabling massive multiplexing density on a single chip.

1.3 Co-Packaged Optics (CPO)

CPO moves the optical transceiver (the laser driver and photodetector) from the front panel of the switch directly onto the same substrate as the compute ASIC (GPU or Switch).

- The Paradigm Shift: The electrical trace length drops from 30+ centimeters (to the front panel) to less than 5 millimeters. The signal integrity is perfect, the power consumption plummets, and the front panel is abolished.

While photons move at the speed of light, integrating photonic generation and modulation onto thermal, logic-focused silicon introduces severe physical constraints.

2.1 The Thermal Resonance Crisis

Micro-Ring Modulators are highly sensitive to temperature. A change of just 1°C can detune the ring by 1nm, ruining its resonance and dropping the optical signal.

- The Flaw: AI ASICs generate massive, fluctuating heat. If an MRM drifts off resonance due to a sudden thermal spike from a heavy matrix multiplication, the optical link dies.
- The Mitigation: CPO architectures MUST integrate localized micro-heaters and thermoelectric coolers onto the MRMs. A closed-loop feedback system constantly applies heat to lock the ring at its resonant wavelength, consuming additional static power.

2.2 The Laser Source Problem

Silicon is an indirect bandgap material—it cannot emit light efficiently. Therefore, the laser source MUST be external.

- The Constraint: High-power, multi-wavelength lasers (necessary for WDM) are fragile and degrade over time. They must be housed off-chip, and their light piped into the silicon waveguides via grating couplers or edge coupling.
- The Impact: If the external laser fails, the entire optical fabric goes dark. CPO architectures require redundant, failover laser arrays.

2.3 The O-E-O Conversion Tax

In current CPO architectures, data leaves the GPU as electricity, is converted to light (E-O), traverses the fiber, is converted back to electricity (O-E), and enters the destination GPU.

- The Flaw: The O-E-O conversion consumes power and adds latency. While better than all-copper links, it is not the optimal end state.

The ultimate evolution of silicon photonics is the elimination of the electrical domain entirely for data transit.

3.1 Optical Network-on-Chip (NoC)

Instead of routing electrical signals through a CPU/ASIC to reach the optical transceiver, the optical waveguides are routed directly to the compute cores.

- The Mechanic: A core generates an electrical signal, which is immediately modulated onto an optical wavelength by a local MRM. The photon travels across the wafer or rack, hits a photodetector at the destination core, and is converted back to an electrical signal directly at the register level.
- The Impact: The electrical interconnect fabric (routers, crossbars) is abolished. Latency drops to the physical speed of light across the die.

3.2 All-Optical Switching (Wavelength Routing)

The holy grail is zero-conversion routing. Data arrives as light, is routed as light, and departs as light, with zero O-E-O conversion in the middle.

- The Mechanic: Utilizing Semiconductor Optical Amplifiers (SOAs) or Mach-Zehnder Interferometers (MZIs), an optical switch can route a specific wavelength to a specific output port based on the wavelength itself, without ever reading the digital 1s and 0s.
- The Impact: A network switch that consumes zero power per bit routed. A 100-Terabit switch becomes a passive prism, directing light rather than processing packets.

The fundamental shift of silicon photonics is the decoupling of bandwidth from power and distance.

- Electrical SerDes: Moving a terabit of data across a rack electrically costs ~15 to 20 picojoules per bit. The power draw is so high it limits the number of links an ASIC can support.
- Silicon Photonics: Moving a terabit of data optically costs < 1 picojoule per bit. The power draw is negligible, allowing an ASIC to support thousands of high-bandwidth optical links.

The Topology Shift: Because electrical signals degrade over distance, GPU clusters are forced into rigid, physical spine-leaf topologies with limited cable lengths. Because optical signals do not degrade over rack-scale distances, silicon photonics enables "flat" topologies. Any GPU can talk to any other GPU with near-zero latency, creating a true, non-blocking, all-to-all supercomputer fabric.

To deploy silicon photonics in production, the Mythos Hardware Standard (MYTHOS-EMT-0004) enforces strict operational and architectural boundaries.

5.1 Mandatory CPO for Scale-Out AI

The Mythos standard prohibits the use of front-panel pluggable optics (QSFP) for scale-out AI fabrics.

- The Mitigation: All AI accelerators (GPUs, NPUs, WSEs) and top-of-rack switches MUST utilize Co-Packaged Optics (CPO). The electrical trace length from ASIC to optical engine MUST NOT exceed 10mm. This guarantees that the power budget is spent on compute, not SerDes.

5.2 AI-Driven Thermal Stabilization

The thermal resonance crisis of MRMs cannot be solved by static PID controllers; AI workloads generate heat too dynamically.

- The Mitigation: The CPO control plane MUST utilize a lightweight, localized AI model (running on an NPU) to predict thermal spikes based on the compute workload. The model pre-heats or pre-cools the MRMs milliseconds before the ASIC temperature shifts, ensuring zero optical link drops.

5.3 The Optical Sovereignty Boundary

Optical links can be physically tapped (e.g., bending a fiber to leak light) without breaking the connection.

- The Mitigation: For sovereign and classified environments, all optical waveguides (both on-die and in-fiber) MUST be physically shielded and monitored. Furthermore, because optical signals can be intercepted, end-to-end encryption (MACsec or PQC MACsec) MUST be applied at the electrical boundary before modulation, ensuring that even if light is tapped, the data remains cryptographically secure.

The strategy of scaling AI bandwidth by pushing more electricity through copper wires has reached the limits of physics. Silicon Photonics proves that the path to exascale AI requires a shift from electrons to photons. By integrating waveguides and modulators directly onto compute silicon, we abolish the SerDes power wall, enable zero-conversion routing, and unlock the flat, all-to-all topologies required for trillion-parameter model training.

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A copper trace is a resistor; a waveguide is a free path.
An electrical SerDes is a power tax; a micro-ring is a whisper.
An O-E-O conversion is a bottleneck; an all-optical switch is a prism.
A front-panel pluggable is a relic; co-packaged optics is the absolute.

The interconnect is the enemy; the photon is the solution.

> Bandwidth may be massive.
> Power-per-bit must be absolute.
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End of Research Note RES-020

9. Source Register

Source	Authority and Status	Freshness Control
OIF Co-Packaging Implementation Agreements https://www.oiforum.com/technical-work/implementation-agreements-ias/	Primary interoperability agreements Living portfolio Published: Living	Validated: 2026-07-22 Review on material revision, withdrawal, supersession, or scheduled report review.

10. Lineage, Review, and Publication Record

Record	Value
Original source file	RES-020_Silicon_Photonics_Chip_to_Chip_Optical_Interconnects.md
Original source words	1568
Upgrade type	Enterprise research report; source and freshness validation; limitations; adoption decision; reproducibility plan
Generated on	2026-07-22
Current status	Candidate Research Report
Publication authority	Formal Mythos approval not yet recorded
Next review	180 days or event-driven trigger, whichever occurs first